Sole Inventor

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Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Kwan Ju KOH**, a citizen of the Republic of Korea, residing at 407-101, Keumkang Maeul, Jung 4-dong, Wonmi-ku, Bucheon-city, Kyungki-do 420-729, Korea have invented new and useful **METHODS OF FORMING A CONTACT HOLE IN A SEMICONDUCTOR DEVICE**, of which the following is a specification.

METHODS OF FORMING A CONTACT HOLE IN A SEMICONDUCTOR DEVICE

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to methods of fabricating semiconductor devices, and more particularly to methods for forming a contact hole or via holes in a semiconductor device by selectively etching a metal insulation film or an interlayer insulation film.

BACKGROUND

[0002] With the trend toward higher and higher integration of semiconductor devices, the width dimension of contact holes or via holes becomes smaller. Accordingly, the aspect ratios of these contact holes or via holes are increasing.

[0003] With the increase of the aspect ratios of the contact holes or the via holes, it becomes more difficult to completely fill the contact hole or the via holes with metal material without leaving any voids.

[0004] Conventional techniques for forming these contact holes in semiconductor devices are described in U.S. Patent 6,551,445, U.S. Patent 6,030,667, U.S. Patent 5,658,425, U.S. Patent 5,302,266, and U.S. Patent 5,189,446.

[0005] Fig. 1 is a sectional view illustrating a conventional method for forming contact holes in a semiconductor device. As shown in that figure, after performing a typical MOS transistor fabrication process for forming a gate 2 of a predetermined width on a silicon wafer 1 defined as an active area

of the device, a silicide 3 is formed on the top surfaces of the gate 2 and the silicon wafer 1 in the active area.

[0006] Next, a metal insulation film 4 is thickly formed on the entire top surface of the silicon wafer 1. The metal insulation film 4 is then planarized by a chemical and mechanical polishing process.

[0007] After a contact hole 100 is formed by selectively etching the metal insulation film 4, a barrier metal film 5 is formed on an inner wall of the contact hole 100. Metal material 6 for filling the contact hole 100 is then formed on the barrier metal film.

[0008] When the metal insulation film 4 is etched by a conventional method, a top edge of the formed contact hole has a shape close to a right angle.

[0009] Because the aspect ratio of the contact hole 100 is relatively large, the barrier metal film 5 is not deposited at a uniform thickness on the inner wall of the contact hole. Accordingly, the barrier metal film 5 is deposited more thickly at an inlet portion of the contact hole 100 than at a deep portion of the contact hole 100 and an overhang occurs.

[0010] Due to the overhang, when the metal material 6 is formed to fill the contact hole 100, the inlet portion of the contact hole 100 is blocked before the deep portion of the contact hole 100 is completely filled. As a result, a void 200, (i.e., an empty space in which the metal material is not filled), remains in the contact hole 100.

[0011] Impurities may enter such a void 200 during subsequent processes. These impurities may result in a fatal error in the operation of the

semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 is a sectional view illustrating a conventional method for forming a contact hole in a semiconductor device.

[0013] Figs. 2a and 2b are sectional views illustrating an example method for forming a contact hole in a semiconductor device in accordance with the teachings of the present disclosure.

DETAILED DESCRIPTION

[0014] Figs. 2a and 2b are sectional views illustrating an example method for forming a contact hole in a semiconductor device. As shown in Fig. 2a, after performing a typical MOS transistor fabrication process for forming a gate 12 of a predetermined width on a silicon wafer 11 defined as an active area of the device, a silicide 13 is formed on the top surfaces of the gate 12 and the silicon wafer 11 in the active area.

[0015] Subsequently, a metal insulation film 14 is thickly formed on the entire top surface of the silicon wafer 11. The metal insulation film 14 is then planarized by a chemical and mechanical polishing process.

[0016] Next, a photosensitive film is applied, exposed and developed on the metal insulation film 14 such that a photosensitive film pattern is formed. The photosensitive film pattern is formed such that the photosensitive film on a region to contain a contact hole is removed. A contact hole 100 is

then formed by dry etching the exposed area of the metal insulation film 14 using the photosensitive film pattern as a mask.

[0017] When the metal insulation film 14 is dry etched, a top edge of the contact hole is rounded by isotropically etching the metal insulation film 14 using a plasma having spiral movement.

[0018] The plasma having spiral movement is widely used in equipment for removal of photosensitive film in process lines. This equipment, which is called an asher, includes equipment having a representative brand name of Ramda-200.

[0019] The principle of this equipment is that charged ions or radicals have spiral movement as the ions or radicals are rotated by a magnetic field. This magnetic field is generated by a coil surrounding a chamber under a state where an electric field is applied vertically downward in the chamber.

[0020] When this equipment is used, gases of the fluorine series can be used as an etching gas.

[0021] Next, as shown in Fig. 2b, a barrier metal film 15 is formed on the entire top surface of the metal insulation film 14 and an inner wall of the contact hole 100. A metal material 16 for filling the contact hole 100 is then formed on the barrier metal film 15.

[0022] Since the top edge of the contact hole 100 is rounded, an inlet portion of the contact hole 100 is widened, thereby preventing generation of an overhang when forming the barrier metal film 15. Accordingly, the contact hole 100 is completely filled with the metal material 16 without creating any voids.

[0023] Although as described above, the illustrated method is applicable to selectively etching a metal insulation film to form a contact hole, the teachings of the present disclosure are also applicable to a case where the interlayer film is selectively etched for the formation of a via hole.

[0024] As described above, when a metal insulation film or an interlayer insulation film is etched to form a contact hole or a via hole, since a top edge of the contact hole or the via hole is rounded by using a plasma having spiral movement, an inlet portion of the contact and/or via hole is widened and generation of an overhang at the inlet when forming the barrier metal film is prevented. Accordingly, the contact and/or via hole is completely filled with metal material without any voids. As a result, defects caused by voids can be prevented, thereby improving the reliability of semiconductor devices.

[0025] From the foregoing, persons of ordinary skill in the art will appreciate that the above disclosed methods prevent voids from being formed in a contact hole or a via hole. To this end, a top edge of a contact hole or a via hole is rounded by using a plasma having spiral movement when a metal insulation film or an interlayer insulation film is etched to form the contact hole or the via hole.

[0026] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.